

# vLA81 User Manual v1.1

As well as providing compatibility with the 2C210E Sinclair ZX81 ULA, the vLA81 also has a few extra functions which can be accessed by the onboard configuration switches. Some configurations are expected to be static (e.g. video settings) while some are programmable by accessing port \$E7 (this port is read/write so the current soft configuration can be both set and read by software when enabled).

## VIDEO MODES

To cater for the various video mods that have evolved over the years there are settings for standard video suitable for directly driving the 75Ω video monitor input or for an extended sync level suitable for the modulator and some video mods which expect it. The back porch can also be disabled, again as some video mods are designed to add a back porch and don't work properly with it present.

### MOD switch

VIDEO MODE	MOD/SW1
1Vp-p into 75Ω	OFF
Extended Sync level	ON

- With SW1 ON and SW2 OFF, the vLA81 emulates a 2C210E.
- With both SW1 and SW2 ON, the vLA81 emulates a 2C158/184.

### BP switch

BACK PORCH	BP/SW2
Enabled	OFF
Disabled	ON

**MIC levels:** As the tape out signal is derived directly from the video output then the MIC level will change dependent on the video configuration. The MOD switch affects this the most with MOD off (75Ω video) providing about half the amplitude of MOD on. The soft configuration modes, Border white/black and normal/inverse video also affect the MIC level. The vLA81 has been tested with several different cassette recorders and all have worked fine although the playback level can be different for different recording levels dependent on how affective the ALC (automatic level control) on the cassette operates.

## MEMORY MODES

Several switched memory configurations are available for those ZX81s with 32K of internal memory (the M1NOT or HIRES mods are not required – see *Fig. 1*). These allow mappings for a standard 16K configuration, the full 32K in two configurations supporting the main HIRES memory schemes (WRX etc.). If an external device, such as the ZXpand or a RAM pack, is connected then any vLA81 memory mappings will be overridden.

### USR0/USR1 switches

MEMORY MAP	USR0/SW3	USR1/SW4
16K-32K	OFF	OFF
16K-48K	ON	OFF
8K-40K	OFF	ON
SOFT CONFIG	ON	ON

## SOFT CONFIGURATION

If the memory configuration (USR0/USR1) switches are both set ON then the software programmable features of the vLA81 are enabled. Additional options available are inverse or normal video, white or black border, and UK or USA video standard. As well as the memory configurations mentioned, the RAM can also be mapped to to the ROM space. This RAM can also be write protected by enabling a write protect bit on the configuration port.

All these soft configurations are lost on power down (note that they are retained on reset) while the video and back porch settings are retained. Any memory configurations set by switches rather than by software are also retained.

### SOFT CONFIGURATION MODE (USR0/USR1 both ON)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	CONFIG PORT(\$E7/dec. 231)
WRPROT	X	X	MEM1	MEM0	USA_UK	BORDER	INVERT	MODE
						0	0	Normal video/White Border
						0	1	Inverse video/White Border
						1	0	Normal video/Black Border
						1	1	Inverse video/Black Border
					0			USA
					1			UK
			0	0				Memory Mode 0 (16K-32K)
			0	1				Memory Mode 1 (16K-48K)
			1	0				Memory Mode 2 (8K-40K)
			1	1				Memory Mode 3 (0K-32K)
0	Page 0 RAM write enable (only valid for MODE 3).							Write Protect
1								Write Enable

#### Notes:

1. In soft config mode, MODE 0 is set by default on power up.
2. The configuration port can only be read when the soft conguration mode is enabled.
3. As all 8 bits are written during a port write, the values to be changed must be combined with the existing configuration to ensure other settings are not altered.
4. Bits 5 and 6 are not used.
5. Write enable is only valid for Page 0 in Mode 3 (see section *vLA Memory Configurations* for more detail).

## vLA81 Memory Configurations

Note: Configurations using [MEM0/MEM1](#) are only available in soft config mode (USR0/USR1 both on).

0000	ROM: D3FD01FF7FC3CB03	
1000	ROM: 9A0DD6C438F901EC	ROM
2000	ROM: D3FD01FF7FC3CB03	
3000	ROM: 9A0DD6C438F901EC	
4000	RAM 4K BYTE	Page 2
5000	RAM 4K BYTE	
6000	RAM 4K BYTE	Page 3
7000	RAM 4K BYTE	
8000	ROM: D3FD01FF7FC3CB03	
9000	ROM: 9A0DD6C438F901EC	
A000	ROM: D3FD01FF7FC3CB03	ROM copy
B000	ROM: 9A0DD6C438F901EC	
C000	MIRROR -RAM	
D000	MIRROR -RAM	Copy of Page 2&3
E000	MIRROR -RAM	
F000	MIRROR -RAM	

MODE 0  
 USR0/SW3 = OFF  
 USR1/SW4 = OFF  
 or  
 MEM0 = 0  
 MEM1 = 0

0000	ROM: D3FD01FF7FC3CB03	
1000	ROM: 9A0DD6C438F901EC	ROM
2000	ROM: D3FD01FF7FC3CB03	
3000	ROM: 9A0DD6C438F901EC	
4000	RAM 4K BYTE	Page 2
5000	RAM 4K BYTE	
6000	RAM 4K BYTE	Page 3
7000	RAM 4K BYTE	
8000	RAM 4K BYTE	Page 0
9000	RAM 4K BYTE	
A000	RAM 4K BYTE	Page 1
B000	RAM 4K BYTE	
C000	MIRROR -RAM	
D000	MIRROR -RAM	Copy of Page 2&3
E000	MIRROR -RAM	
F000	MIRROR -RAM	

MODE 1  
 USR0/SW3 = ON  
 USR1/SW4 = OFF  
 or  
 MEM0 = 1  
 MEM1 = 0

0000	ROM: D3FD01FF7FC3CB03	
1000	ROM: 9A0DD6C438F901EC	ROM
2000	RAM 4K BYTE	Page 1
3000	RAM 4K BYTE	
4000	RAM 4K BYTE	Page 2
5000	RAM 4K BYTE	
6000	RAM 4K BYTE	Page 3
7000	RAM 4K BYTE	
8000	RAM 4K BYTE	Page 0
9000	RAM 4K BYTE	
A000	ROM: D3FD01FF7FC3CB03	ROM copy
B000	ROM: 9A0DD6C438F901EC	
C000	MIRROR -RAM	
D000	MIRROR -RAM	Copy of Page 2&3
E000	MIRROR -RAM	
F000	MIRROR -RAM	

MODE 2  
 USR0/SW3 = OFF  
 USR1/SW4 = ON  
 or  
 MEM0 = 1  
 MEM1 = 0

0000	RAM 4K BYTE	
1000	RAM 4K BYTE	Page 0
2000	RAM 4K BYTE	
3000	RAM 4K BYTE	Page 1
4000	RAM 4K BYTE	
5000	RAM 4K BYTE	Page 2
6000	RAM 4K BYTE	
7000	RAM 4K BYTE	Page 3
8000	ROM: D3FD01FF7FC3CB03	
9000	ROM: 9A0DD6C438F901EC	
A000	ROM: D3FD01FF7FC3CB03	ROM copy
B000	ROM: 9A0DD6C438F901EC	
C000	MIRROR -RAM	
D000	MIRROR -RAM	Copy of Page 2&3
E000	MIRROR -RAM	
F000	MIRROR -RAM	

MODE 3  
 USR0/SW3 = ON  
 USR1/SW4 = ON  
 MEM0 = 1  
 MEM1 = 1

1. Mode 0 is the standard memory configuration for an unmodified ZX81.
2. Mode 1 provides an upper 32K memory map and support for HIRES programs.
3. Mode 2 provides a lower 32K memory map suitable for WRX HIRES programs.
4. Mode 3 provides a zero based 32K memory map that can have a patched ROM active. Requires internal 32K with A13 connected to ULA socket pin 35 (see section of internal 32K memory expansion).

Memory maps courtesy of SYSINFO.

## INTERNAL 32K MEMORY EXPANSION

The vLA81 supports 32K of static SRAM (62256 or equivalent) connected directly to the Z80 bus. There is no need for the M1NOT or HIRES mods and if they are present they need to be removed.

To enable Memory MODE 3, A13 needs to be connected to pin 35 of the ULA socket to provide extended memory decoding. Pin 35 normally provides a connection to the 3.5MHz ceramic resonator for the original ULA but as the vLA81 has it's own oscillator the pin can be used for another function. Note that if the original ULA is installed then then A13 will need to be removed from ULA-pin 35.

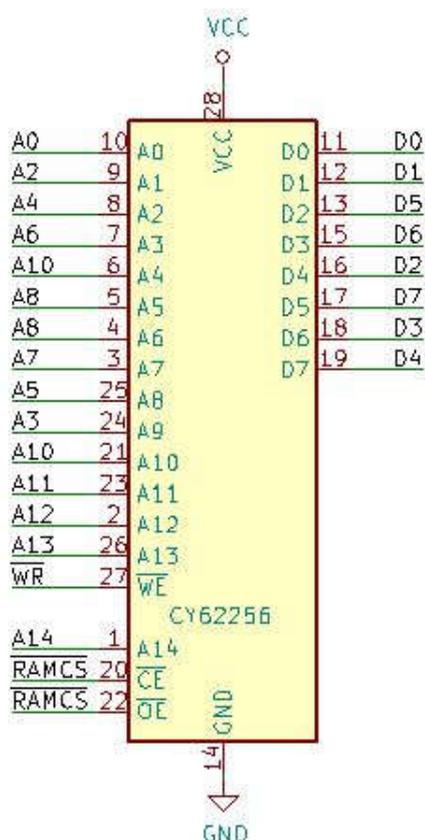


Fig. 1 ZX81 Internal 32K RAM Schematic

## HOW TO COPY THE ROM (some assembly required)

This procedure is only valid for internal 32K memory as described above with no memory overriding expansions connected.

1. Set the USR0 and USR1 both ON to enable the soft configuration mode.
2. Set the memory mode to MODE 1 (default is MODE 0). This places the start of PAGE 0 at \$8000.
3. Copy the patched ROM image to PAGE 0 (starting at \$8000).
4. Set the memory mode to MODE 3. This moves the PAGE 0 start address to \$0000.
5. The WRPROT config bit is normally set to enabled (no write). To change the contents of the ROM space set the WRPROT bit to 1. Remember to change it back after any patching as code could be overwritten!

### Code Example:

```
ld c,231           ;ULA config port
push bc           ;save config port
ld a,%00001000    ;switch to 16K-48K map
out (c),a         ;page 0 now starts at address 32768
ld hl,ROMSTART    ;rom start
ld bc,8192        ;rom length
ld de,32768       ;write to start of page 0
ldir              ;copy rom
pop bc            ;restore config port
ld a,%10011000    ;now switch to 0K-32K map and enable write
out (c),a         ;page 0 magically now starts at address 0
ret
```

This could be improved by first reading the config port to determine the current configuration and only changing the bits required. I'll leave that to you!